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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/099,707 | 03/13/2002 | Stjepan W. Andrasic | 174/223 | 2004 |

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| EXAMINER | |
|---|---|
| LAM, TUAN THIEU | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2816 | |

DATE MAILED: 11/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/099,707 | ANDRASIC ET AL. | |
| | Examiner | Art Unit | |
| | Tuan T. Lam | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *17 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,3-12 and 14-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11,12 and 14-16* is/are allowed.

6)☒ Claim(s) *1,3-6 and 17-26* is/are rejected.

7)☒ Claim(s) *7-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

This is a response to the amendment filed 9/17/2003. Claims 1, 3-12 and 14-26 are pending.

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3-6 and 17-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Tsai et al. (USP 6,157,266), prior art of record.

Figure 1A shows a variable delay cell comprising a plurality of load resistance transistors (first signal controlled active load and details shown in figure 1B) connectable in parallel with one another, a plurality of bias current transistors (first signal controlled and second controlled current sources) connectable in parallel with one another, a switching transistor (one transistor of the differential pair of transistors) connected in series between the plurality of load resistance transistors and the plurality of bias current transistors, switching circuitry (not shown) for producing control signals VCO_P and Bias_P selectively connect one of the load resistance transistors in parallel with at least one other of the load resistance transistor, and further switching circuitry (not shown) producing control signals VCO_N and BIAS_N selectively connected at one of the bias current transistors in parallel with at least one other of the bias current transistors as called for in claims 1 and 17-19.

Regarding claim 3, the further load resistance transistors are seen the transistors of the second controlled active load, the further switching transistor (the other transistor of the differential pair of transistors.

Regarding claim 4, the further load resistance transistors are selectively connected in parallel by the control signals VCO_P and BIAS_P.

Regarding claims 5-6, the switching circuitry and the further switching circuitry are programmable to generate control signals.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai et al. (USP 6,157,266) in view of Horan et al. (USP 6,462,623), both prior art of record. Figure 1A shows a variable delay cell comprising a plurality of load resistance transistors (first signal controlled active load and details shown in figure 1B) connectable in parallel with one another, a plurality of bias current transistors (first signal controlled and second controlled current sources) connectable in parallel with one another, a switching transistor (one transistor of the differential pair of transistors) connected in series between the plurality of load resistance transistors and the plurality of bias current transistors, switching circuitry (not shown) for producing control signals VCO_P and Bias_P selectively connect one of the load resistance transistors in parallel with at least one other of the load resistance transistor, and further switching circuitry (not shown)

producing control signals VCO_N and BIAS_N selectively connected at one of the bias current transistors in parallel with at least one other of the bias current transistors.

The difference seen between Tsai et al. and the present invention is the arrangement of an oscillator forming a phase locked loop as called for in claims 19-22. Horan et al. teaches the usage of an oscillator in the circuit arrangement of a phase locked loop for providing an accurate output. Therefore, it would have been obvious to a person skilled in the art at the time of the invention was made to use Tsai et al.'s oscillator in a phase locked loop to provide an accurate clock signal.

Claims 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai et al. (USP 6,157,266). Tsai et al. reference discloses all the aspects of the present invention as noted above except for coupling the programmable logic device to a processor and a memory device in a digital processing system as called for in claim 23. However, it is notoriously well known in the art that digital processing system, i.e., microcomputer, commonly consisting of a processor, a memory and programmable logic device (clock generator) coupled to the processor and the memory to insure a synchronous operation in transferring data in or out to or from the components. Therefore, it would have been obvious to a person skilled in the art at the time of the invention was made to use the programmable logic device in a digital processing system to provide a synchronous operation between components thus ensuring erroneous free operative device.

Regarding claim 24, since an integrated circuit manufactured by mass production is readily available and inexpensive, one skilled in the art would have been taken to realize mounting the integrated circuit on a printed circuit board to minimize the cost of producing.

Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to mount the integrated programmable logic device on a printed circuit board for the purpose of minimizing cost of producing.

Regarding claims 25-26, Tsai et al. reference discloses all the aspects of the present invention as noted above except for coupling the programmable logic device to a processor and a memory device in a digital processing system as called for in claims 25-26. However, it is notoriously well known in the art that digital processing system, i.e., microcomputer, commonly consisting of a processor, a memory and programmable logic device (clock generator) coupled to the processor and the memory to insure a synchronous operation in transferring data in or out to or from the components. Therefore, it would have been obvious to a person skilled in the art at the time of the invention was made to use the programmable logic device in a digital processing system to provide a synchronous operation between components thus ensuring erroneous free operative device.

***Allowable Subject Matter***

4. Claims 7-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claims 11-12 and 14-16 are presently allowed.

6. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to teach or fairly suggest switching circuitry and further switching circuitry selectively configured to selectively apply either a substantially fixed deactivating control signal or a variable activating control signal to at least one of the load resistance transistors.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 703-305-3791. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P CALLAHAN can be reached on 730-308-4876. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Tuan T. Lam
Primary Examiner
Art Unit 2816

11/5/2003